Please amend claims 1, 2, 4, 5, 7, 8, 12 and 13 as follows. Pursuant to 37 C.F.R. § 1.121, as amended, a copy of the marked-up version of the original claim is attached to this Response showing the changes made therein.

1. (Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit.

2. (Amended) The microprocessor according to claim 1, wherein when said load module stored in said first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

4. (Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a processing unit which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit.

5. (Amended) The microprocessor according to claim 4, wherein when said load module stored in said first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

7. (Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memories to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit.

8. (Amended) The memory device according to claim 7, wherein when said load module stored in said first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

12. (Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a processing unit means which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit.

13. (Amended) The memory device according to claim 12, wherein when said load module stored in said first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

REMARKS

The Office Action dated May 13, 2002 has been received and carefully noted. The above amendments and following remarks are submitted as a full and complete response thereto.

Claims 1-16 are pending. By this Response, claims 1, 2, 4, 5, 7, 8, 12 and 13 have been amended. No new matter has been added by the new claims or the amendments . Therefore, claims 1-16 are respectfully submitted for consideration.

Claims 2, 4, 5, 8, 12 and 13 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.